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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,864	03/30/2004	David Sinai	P-6641-US	3802

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EITAN, PEARL, LATZER & COHEN ZEDEK LLP
10 ROCKEFELLER PLAZA, SUITE 1001
NEW YORK, NY 10020

EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,864	SINAI, DAVID	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-16 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohtsuka(US Patent 5,809,315).

As to claim 1, Ohtsuka discloses a method comprising setting an operating voltage(detection voltage, see column 5, line 56) supplied to a processor(voltage detection means 2, see Fig. 1) based on a mode of operation(operation mode, see column 5, line 53) of the processor(see column 5, lines 52-57).

As to claim 2, Ohtsuka discloses the method comprising determining an actual mode of operation of the processor, wherein setting comprises setting the operating voltage based on the actual mode of operation(see column 5, lines 52-57).

As to claim 3, Ohtsuka discloses the method wherein determining comprises sensing a level of power supplied to the processor(see column 5, lines 57-60).

As to claim 4, Ohtsuka discloses the method comprising receiving a signal indicating an anticipated mode of operation of the processor, wherein setting comprises setting the operating voltage based on the signal(see column 5, lines 52-57; and column 6, lines 27-37).

As to claim 5, Ohtsuka discloses the method comprising reducing the operating voltage when the mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 6, Ohtsuka discloses the method comprising reducing the operating voltage when the actual mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 7, Ohtsuka discloses the method comprising reducing the operating voltage in response to the signal when the anticipated mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 8, Ohtsuka discloses the method comprising increasing the operating voltage when the signal indicates that the processor is about to go out of sleep mode(see column 6, lines 2-4).

As to claim 9, Ohtsuka discloses an apparatus comprising a controller(control means 4, see Fig. 1) to set an operating voltage(detection voltage, see column 5, line 56) supplied to a processor(voltage detection means 2, see Fig. 1) based on a mode of operation(operation mode, see column 5, line 53) of the processor(see column 5, lines 52-57).

As to claim 10, Ohtsuka discloses the apparatus wherein the controller is able to determine an actual mode of operation of the processor and to set the operating voltage based on the actual mode of operation(see column 5, lines 52-57).

As to claim 11, Ohtsuka discloses the apparatus wherein the controller is able to sense a level of power supplied to the processor(see column 5, lines 57-60).

As to claim 12, Ohtsuka discloses the apparatus wherein the controller is able to receive a signal indicating an anticipated mode of operation of the processor and to set

the operating voltage based on the signal(see column 5, lines 52-57; and column 6, lines 27-37).

As to claim 13, Ohtsuka discloses the apparatus wherein the controller is able to reduce the operating voltage when the mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 14, Ohtsuka discloses the apparatus wherein the controller is able to reduce the operating voltage when the actual mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 15, Ohtsuka discloses the apparatus wherein the controller is able to reduce the operating voltage in response to the signal when the anticipated mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 16, Ohtsuka discloses the apparatus of claim 12, wherein the controller is able to increase the operating voltage when the signal indicates that the processor is about to go out of sleep mode(see column 6, lines 2-4).

As to claim 25, Ohtsuka discloses a machine-readable medium having stored thereon a set of instructions that, if executed by a machine, cause the machine to perform a method comprising setting an operating voltage(detection voltage, see column 5, line 56) supplied to a processor(voltage detection means 2, see Fig. 1) based on a mode of operation(operation mode, see column 5, line 53) of the processor(see column 5, lines 52-57).

As to claim 26, Ohtsuka discloses the machine-readable medium wherein the instructions result in determining an actual mode of operation of the processor, and

wherein the instructions that result in setting result in setting the operating voltage based on the actual mode of operation(see column 5, lines 52-57).

As to claim 27, Ohtsuka discloses the machine-readable medium wherein the instructions result in receiving a signal indicating an anticipated mode of operation of the processor, and wherein the instructions that result in setting result in setting the operating voltage based on the signal(see column 5, lines 52-57; and column 6, lines 27-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtsuka(US Patent 5,809,315) further in view of Shteyn et al.(US PGPub 2003/0040344).

As to claim 17, a device comprising a processor(voltage detection means 2, see Fig. 1), a controller(control means 4, see Fig. 1) to set an operating voltage(detection voltage, see column 5, line 56) supplied to the processor based on a mode of operation(operation mode, see column 5, line 53) of the processor(see column 5, lines 52-57). However, Ohtsuka fails to disclose a device being a wireless communication device comprising a dipole antenna to send and receive wireless communication signals.

Shteyn discloses a wireless communication device(communicator 102) comprising a dipole antenna(antenna, see paragraph 0008, line 9) to send and receive wireless communication signals. It would have been obvious to combine the inventions of Ohtsuka and Shteyn in order to create a wireless communication device with abilities to detect a mode of operation and from that information adjust an operating voltage. The motivation to do so would be to conserve power of the device over a wireless network.

As to claim 18, Ohtsuka discloses the device wherein the controller is able to determine an actual mode of operation of the processor and to set the operating voltage based on the actual mode of operation(see column 5, lines 52-57).

As to claim 19, Ohtsuka discloses the device wherein the controller is able to sense a level of power supplied to the processor(see column 5, lines 57-60).

As to claim 20, Ohtsuka discloses the device wherein the controller is able to receive a signal indicating an anticipated mode of operation of the processor and to set

the operating voltage based on the signal(see column 5, lines 52-57; and column 6, lines 27-37).

As to claim 21, Ohtsuka discloses the device wherein the controller is able to reduce the operating voltage when the mode of operation is a sleep mode(see column 6, lines 2-4).

As to claim 22, Ohtsuka discloses a device comprising a processor(voltage detection means 2, see Fig. 1), a controller(control means 4, see Fig. 1) to set an operating voltage(detection voltage, see column 5, line 56) supplied to the processor based on a mode of operation(operation mode, see column 5, line 53) of the processor(see column 5, lines 52-57); and a dipole antenna to send and receive wireless communication signals. However Ohtsuka fails to disclose the device being part of a wireless communication system comprising a first wireless communication device and a second wireless communication device comprising a dipole antenna to send and receive wireless communication signals.

Shteyn discloses a wireless communication system(system 100, see Fig. 1) comprising a first wireless communication device(communicator 104, see Fig. 1), and a second wireless communication device(communicator 102, see Fig. 1)) comprising a dipole antenna(antenna, see paragraph 0008, line 9) to send and receive wireless communication signals. It would have been obvious to combine the inventions of Ohtsuka and Shteyn in order to create a wireless communication system with abilities to detect a mode of operation of a wireless device and from that information adjust the

operating voltage. The motivation to do so would be to conserve power of the device over a wireless network.

As to claim 23, Ohtsuka discloses system wherein the controller is able to determine an actual mode of operation of the processor and to set the operating voltage based on the actual mode of operation(see column 5, lines 52-57).

As to claim 24, Ohtsuka discloses the system wherein the controller is able to receive a signal indicating an anticipated mode of operation of the processor and to set the operating voltage based on the signal(see column 5, lines 52-57; and column 6, lines 27-37).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100